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CNF			<p><b><u>Flash memory BIOS for PC and notebook computers</u></b>  Jex, J.  Communications, Computers and Signal Processing, 1991., IEEE Pacific Rim Conference on , 1991 , Page(s): 692 -695 vol.2</p>
CNF			<p><b><u>Row-redundancy scheme for high-density flash memory</u></b>  Mihara, M.; Nakayama, T.; Ohkawa, M.; Kawai, S.; Miyawaki, Y.; Terada, Y.; Ohi, M.; Onoda, H.; Ajika, N.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.  Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International , 1994 , Page(s): 150 -151</p>
CNF			<p><b><u>A high density NAND EEPROM with block-page programming for microcomputer applications</u></b>  Momodomi, M.; Iwata, Y.; Tanaka, T.; Itoh, Y.; Shirota, R.; Masuoka, F.  Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989 , 1989 , Page(s): 10.1/1 -10.1/4</p>
PER			<p><b><u>A quick intelligent page-programming architecture and a shielded bitline sensing method for 3 V-only NAND flash memory</u></b>  Tanaka, T.; Tanaka, Y.; Nakamura, H.; Sakui, K.; Oodaira, H.; Shirota, R.; Ohuchi, K.; Masuoka, F.; Hara, H.  Solid-State Circuits, IEEE Journal of Volume: 29 11 , N v. 1994 , Page(s): 1366 -1373</p>
CNF			<p><b><u>A 35 ns-cycle-time 3.3 V-only 32 Mb NAND flash EEPROM</u></b>  Imamiya, K.; Iwata, Y.; Sugiura, Y.; Nakamura, H.; Oodaira, H.; Momodomi, M.; Ito, Y.; Watanabe, T.; Araki, H.; Narita, K.; Masuda, K.; Miyamoto, J.  Solid-State Circuits Conference, 1995. Digest of Technical Papers. 41st ISSCC, 1995 IEEE International , 1995 ,</p>

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CNF



**A 3.3 V-only 16 Mb DINOR flash memory**

*Kobayashi, S.; Mihara, M.; Miyawaki, Y.; Ishii, M.; Futatsuya, T.; Hosogane, A.; Ohba, A.; Terada, Y.; Ajika, N.; Kunori, Y.; Yuzuriha, K.; Hatanaka, M.; Miyoshi, H.; Yoshihara, T.; Uji, Y.; Matsuo, A.; Taniguchi, Y.; Kiguchi, Y.*

Solid-State Circuits Conference, 1995. Digest of Technical Papers. 41st ISSCC, 1995 IEEE International , 1995 ,  
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**New submicron non-volatile memory modules for 16/32-bit devices**

*Kuo, C.; Morton, B.; Toms, T.; Weidner, M.; Chudimsky, D.; Choe, H.; Bowers, M.; Yeon-seuk Kim; Chang, K.M.; Smith, P.*

VLSI Technology, Systems, and Applications, 1993.  
Proceedings of Technical Papers. 1993 International Symposium on , 1993 , Page(s): 343 -347

CNF



**A 1 Mbit EEPROM with MONOS memory cell for semiconductor disk application**

*Nozaki, T.; Tanaka, T.; Kijiyu, Y.; Kinoshita, E.; Tsuchiya, T.; Hayashi, Y.*

VLSI Circuits, 1990. Digest of Technical Papers., 1990 Symposium on , 1990 , Page(s): 101 -102

PER



**A 35 ns cycle time & 3 V only 32 Mb NAND flash EEPROM**

*Iwata, Y.; Imamiya, K.; Sugiura, Y.; Nakamura, H.; Oodaira, H.; Momodomi, M.; Itoh, Y.; Watanabe, T.; Araki, H.; Narita, K.; Masuda, K.; Miyamoto, J.-I.*

Solid-State Circuits, IEEE Journal of  
Volume: 30 11 , Nov. 1995 , Page(s): 1157 -1164

PER



**A 60-ns 16-Mb flash EEPROM with program and erase sequence controller**

*Nakayama, T.; Kobayashi, S.; Miyawaki, Y.; Terada, Y.; Ajika, N.; Ohi, M.; Arima, H.; Matsukawa, T.; Yoshihara, T.; Suzuki, K.*

Solid-State Circuits, IEEE Journal of  
Volume: 26 11 , Nov. 1991 , Page(s): 1600 -1605

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